THE DESIGN AND PERFORMANCE OF A DOUBLE BALANCED MIXER USING FETs

S.J. NIGHTINGALE, M.A.G. UPTON AND N.V. DANDEKAR

GENERAL ELECTRIC COMPANY, ELECTRONICS LABORATORY, SYRACUSE, NY 13221

Abstract

A new theoretical approach has been developed to analyze and design a double balanced mixer using FETs. This approach also enables single ended and single balanced mixer designs to be analyzed. Theoretical and practical results will be presented for a wideband (6-18 GHz) double balanced mixer for EW applications.

Introduction

A theory has been developed to analyze both wide and narrow band double balanced mixers using any device which can be represented as a 2-port element, e.g., FET, HEMT, diode, etc. A general block diagram of the double balanced mixer is given in Figure 1a. The circuit comprises 180 degree phase splitters for signal and LO and a commutator circuit which performs the frequency conversion. The mixer analysis has been used to design a wideband (6-18 GHz) double balanced mixer for EW applications and narrow band mixers (36-38 GHz) for communication applications. The analysis enables phase and magnitude imbalances in both the LO and signal circuits to be considered and any device imbalances in the commutator circuit. The performance can then be evaluated in terms of conversion gain/loss, input and output impedances and port to port isolation for any signal or sideband frequency.

The mixer analysis has been developed using the theory of linear circuits with time varying parameters. This analysis technique relies on the assumption that the local oscillator is much larger than the input signal and is therefore solely responsible for changing the impedance of a nonlinear device in a time-varying periodic manner. Accepting this assumption, it is then possible to analyze the circuit in 2 stages. Firstly, a large signal nonlinear analysis is performed to determine the harmonic voltages and currents present in the circuit and hence the time varying impedances. Secondly, using these time varying impedances, a small signal analysis is performed to calculate the conversion gain, input and output impedances and port to port isolation.

The analysis developed uses a bilinear model for the commutator circuit. This model assumes that the device switches between 2 levels at the local oscillator frequency. It has already been shown from work with diodes that the bilinear or pulse approximation is valid under medium to strong pumping conditions. However, the analysis could be readily modified to incorporate the time varying impedance derived from a more general treatment if required. The pumped commutator is defined by 5 real and 16 complex parameters for each signal or mixed product frequency under investigation. Each half can be specified by the S-parameters in the "on" and "off" states (8 complex), a pulse duty ratio (1 real) which defines the time spent in the on state and a rise time (1 real) which defines the transition between the on and off states. A phase error term (1 real) defines the departure from antiphase pumping of the 2 halves. The signal and LO splitters are completely defined by 3 port S-parameters (12 complex each).

A special technique was developed to analyze the mixer using S, ABCD and Y parameters to determine 4 overall admittance functions. These functions enabled the currents to be found in the source and load impedances when the mixer was driven from the signal and IF port. Deriving each of these admittance functions for the 4 commutator states enabled 4 new variables to be found which were used to define the Fourier series admittance waveforms. Four sets of Fourier series were found corresponding to each of the conditions mentioned above for each frequency in the commutator. Appropriate cross-multiples of the terms of the Fourier series enabled the currents at the signal and different mixed product frequencies to be calculated to determine conversion gain/loss, input and output impedances and port to port isolation for any signal or sideband frequency.

The overall procedure is quite complex and a computer program has been written which incorporates all of the analysis theory.

Simple Example: Diode Lattice Mixer

After completing a series of tests on the program, the mixer circuit given in Figure 1a was analyzed. This circuit is equivalent in many respects to the lattice mixer shown underneath in 1b. The circuit considered has infinite bandwidth and the phase splitter has 3 dB gain. A perfect switch (represented in the program by a very high or a very low impedance value) provides the time varying admittance which performs the frequency conversion process. Since any part of the circuit has constant gain with frequency, the analysis for this simple circuit predicts a somewhat higher value for the higher order mixed products than would be the case in any practical circuit. However, the circuit given provides valuable insight into what happens when the different circuit parameters are varied. Figures 2 to 5 show the variation in conversion loss and RF/IF mutual isolation as a function of pulse duty ratio imbalance, RF phase splitter error, LO phase splitter error and RF phase splitter gain imbalance. Additional features are given in Table 1. As far as we are aware, no previous works have shown the results given here.

Wideband FET Mixer

A monolithic wideband (6-18 GHz) double balanced mixer was designed using FETs and the performance calculated and optimized using the computer program just described.

The theoretical conversion gain of the complete mixer circuit is shown in Figure 6. This curve was calculated while maintaining a constant IF of 2 GHz and shows a conversion gain of 3 dB $\pm$ 2 dB from 6-18 GHz. The input and output VSWRs are shown in Figure 7. The input VSWR is virtually independent of the LO frequency and is better than 1.8:1 over 6-18 GHz. The output VSWR is shown to be less than 2:1 for a constant IF of 2 GHz as the frequency is varied from 6-18 GHz.

Mixer Fabrication

The wideband mixer chips were fabricated using our 0.5 micron process for GaAs MMICs. The process features photolithographically defined 0.5 micron gates, thin MIM capacitors, semiconductor resistors fabricated in the active layer, plated air bridge crossovers and interconnects and via hole grounding. Commercially available VPE material was used where the epitaxial layers were specified to have n^+ doping for the contact layer and 2.5×10^{17} doping for the active layer. All lithography was performed using the contact aligners and the steps which involve metallization and lift-off technique made use of a deep UV double-layer resist method to pattern the resist. In particular, the fabrication of 0.5 micron gate fingers by E-beam metallization and lift-off utilize the latter technique.

The processing sequence begins with an anodic etch of the channel regions. This enables uniform electrical characteristics for the active layer to be achieved across the wafer. Active regions for the MESFETs and the resistors are isolated by mesa-etch, then ohmic contacts are formed by AuGeNi metallization and rapid thermal annealing. The Ti/Pt/Au gate metal is evaporated by E-beam after recessing the gate region to achieve a pinchoff voltage of 3.5 volts. Next, capacitor bottom plates in the MIM structures are formed, along with the transmission lines, by metallization and lift-off technique. The nitride layer is deposited by the plasma CVD technique, and is patterned by CF_4 etching. Apart from forming the MIM capacitors, the nitride also protects the device channels and the active layer resistors. The top plate for the capacitors and the air bridges are formed in the plating step when the transmission lines and interconnects are also Au plated to a thickness of 2.5 microns. Figures 8 and 9 show SEM views of two 0.5 micron gate MESFETs, with 150 and 500 micron widths, which

0149-645X/85/0000-0717 $01.00 © 1985 IEEE

comprise active elements in the mixer circuit. Figure 9 also shows an example of the active layer resistor, MIM capacitors and air bridge crossovers.

Following the frontside processing, wafers are thinned to 100 microns. Wet etched vias are fabricated which involve the use of an IR aligner. Each mixer chip has 14 vias providing a connection to ground at various points in the circuit. In the interests of keeping a high yield of working chips in this program, we chose a circuit layout which did not allow a via-hole directly under a MIM capacitor.

Finally, a special mention is due for the deep UV double resist technique which enables the necessary resolution and yield for the 0.5 micron gate fingers to be achieved. The linewidth variation at 0.5 micron feature size is presently limited by the linewidth variation originating in the 1 x 1 mask itself. Because of the high quality of gate-pattern transferred from mask onto the wafer, we are able to achieve uniformity in the gate-recess etch. The latter in turn leads to uniform I_{dss} and other characteristics for the MESFETs in the mixer circuit.

A photograph of the die is given in Figure 10 showing two complete mixer circuits (size 1.3 x 5 mm) and separate parts of the complete mixer together with discrete devices and a TEG. To date, wafers have been processed yielding over 500 complete mixer circuits together with component parts of the mixer circuit and discrete devices.

DC and RF Testing

Several discrete devices from the first lot have been characterized prior to measuring the complete circuit. Amplifier data derived from the measured S-parameters indicates a gain of 13 dB at 18 GHz from an 0.5 x 150 micron "T" gate FET. The mixer circuits are currently being tested and measured results will be presented and discussed during the Conference.

Several specially designed test fixtures have been developed for characterizing the phase splitters and commutator as well as the complete mixer circuit. Figure 11 shows the test fixture for the commutator. The chip is mounted in a carrier shown on the RHS. This is inserted into the main test fixture from the underside and the DC and RF connections are made with Au ribbons. The ribbons are bonded to the main substrate and make a demountable pressure contact to the carrier by means of a rexolite ring which exerts pressure on the ribbon from above.

Conclusion

An approach to analyzing a FET double balanced mixer has been described and some test results presented showing the effect of varying the parameter values used in the mixer building block. The design described was shown to be very tolerant to circuit variations and has been realized in monolithic form on GaAs.

Acknowledgments

This work is sponsored by the Electronics Technology and Devices Laboratory, Fort Monmouth, NJ 07703 under Contract No. DAAK20-83-C-0416.

The authors wish to acknowledge Mary Pyle for her technical assistance.

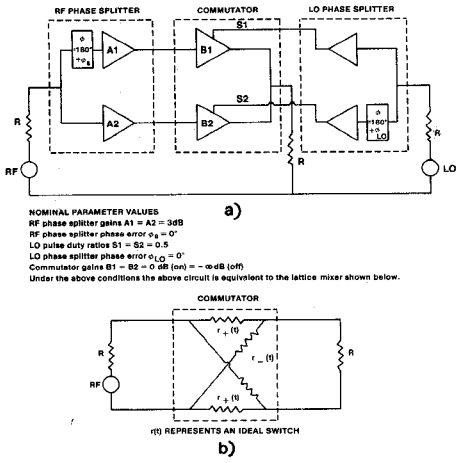

FIGURE 1. BLOCK DIAGRAM OF WIDEBAND DOUBLE BALANCED MIXER CIRCUIT

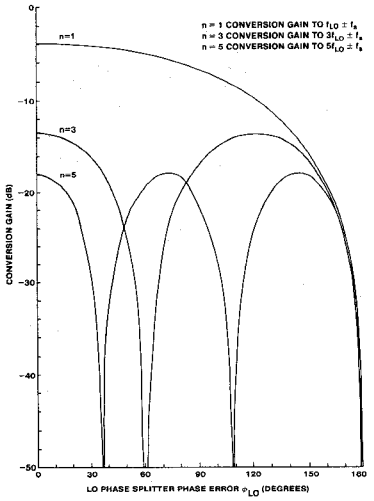

FIGURE 2. CONVERSION GAIN VERSUS LO PHASE SPLITTER PHASE ERROR

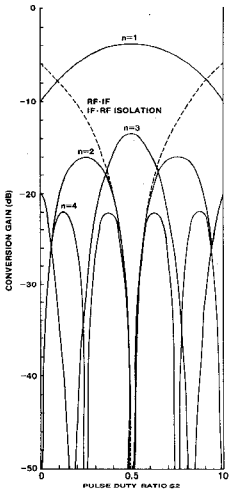

FIGURE 3. CONVERSION GAIN VERSUS LO PULSE DUTY RATIO IMBALANCE

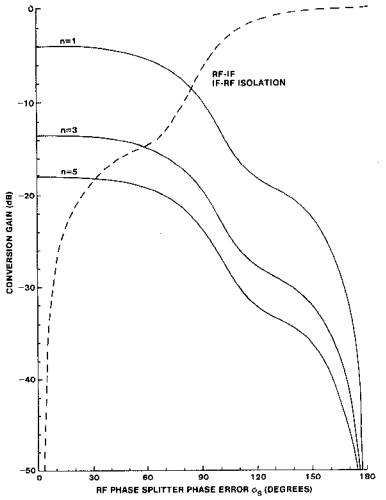

FIGURE 4. CONVERSION GAIN VERSUS RF PHASE SPLITTER PHASE ERROR

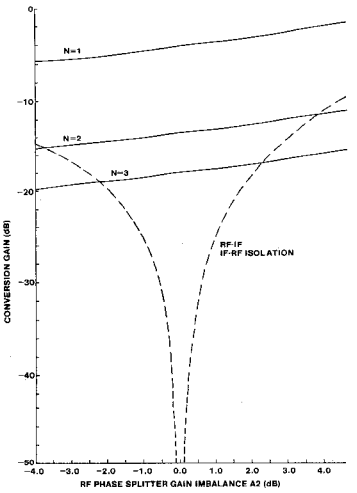

FIGURE 5. CONVERSION GAIN VERSUS RF PHASE SPLITTER GAIN IMBALANCE

Figure 2

A1 = 3 dB A2 = 3 dB $\phi_s = 0°$ S1 = 0.5 S2 = 0.5 ϕ_{LO} = varied

Key Features

1) The input and output are matched for all ϕ_{LO} (not shown).
2) No even order mixed products are generated for any ϕ_{LO}.
3) Infinite RF-IF and IF-RF isolation is maintained for any ϕ_{LO}.
4) As ϕ_{LO} varies from 0°-180° the mixer operation changes from a transmission circuit to a reflection circuit (i.e., when $\phi_{LO} = 180°$ all the odd order mixed products are dissipated in the signal source impedance.)

Figure 3

A1 = 3 dB A2 = 3 dB $\phi_s = 0°$ S1 = 0.5 S2 = varied $\phi_{LO} = 0°$

Key Features

1) The input and output impedances are always real and vary from 3R at S2 = 0 to $\frac{R}{3}$ at s = 1 with a match at S2 = 0.5.
2) Odd and even order mixed products are present.
3) The RF-IF and IF-RF isolation varies from 6 dB at S2 = 0 to ∞ dB at S2 = 0.5 to 6 dB at S2 = 1.

Figure 4

A1 = 3 dB A2 = 3 dB ϕ_s = varied S1 = 0.5 S 2 = 0.5 $\phi_{LO} = 0°$

Key Features

1) The input and output are matched only at $\phi_{LO} = 0$ and 180°, the impedances are in general complex, but equal $\frac{R}{3}$ when $\phi_{LO} = 90°$.
2) No even order mixed products are generated.
3) The RF-IF and IF-RF isolation decreases from ∞ at $\phi_{LO} = 0$ to 0 at $\phi_{LO} = 180°$.
4) At $\phi_{LO} = 180°$ no frequency conversion takes place and half the available input power is dissipated in the load resistor and half in the source resistor.

Figure 5

A1 = 3 dB A2 - varied $\phi_s = 0°$ S1 = 0.5 S2 = 0.5 $\phi_{LO} = 0°$

Key Features

1) The input and output are matched for all values of gain imbalance.
2) No even order products are generated.
3) There is a constant power difference between the odd order mixed products as the gain imbalance is varied.
4) The RF-IF and IF-RF isolation decreases from ∞ with increasing gain imbalance.

TABLE 1. ADDITIONAL FEATURES RELEVANT TO FIGURES 2 TO 5

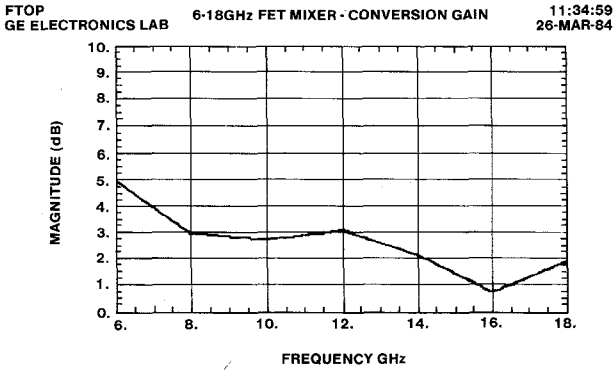

FIGURE 6 CONVERSION GAIN OF WIDEBAND DOUBLE BALANCED MIXER

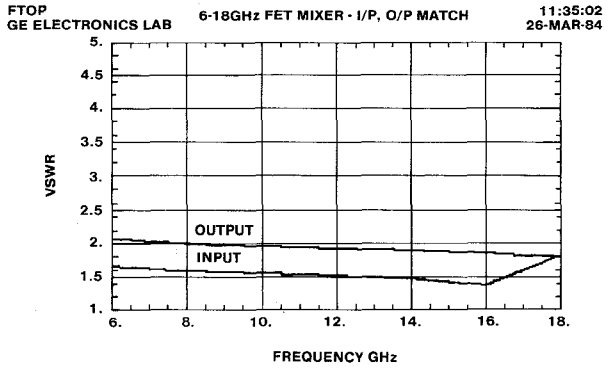

FIGURE 7 INPUT AND OUTPUT VSWR OF WIDEBAND DOUBLE BALANCED MIXER

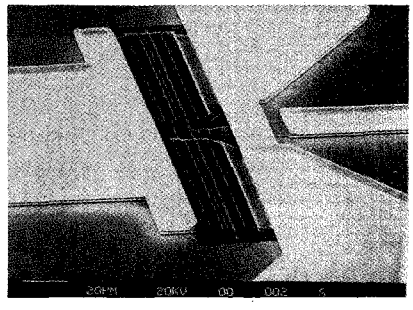

FIGURE 8 SEM VIEW OF 150 MICRON GaAs FET

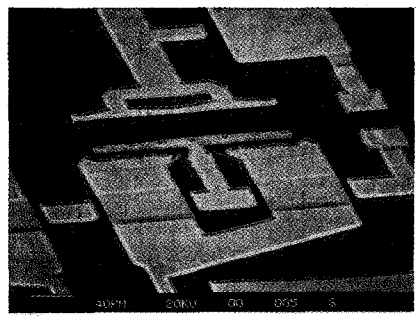

FIGURE 9 SEM VIEW OF 500 MICRON GaAs FET

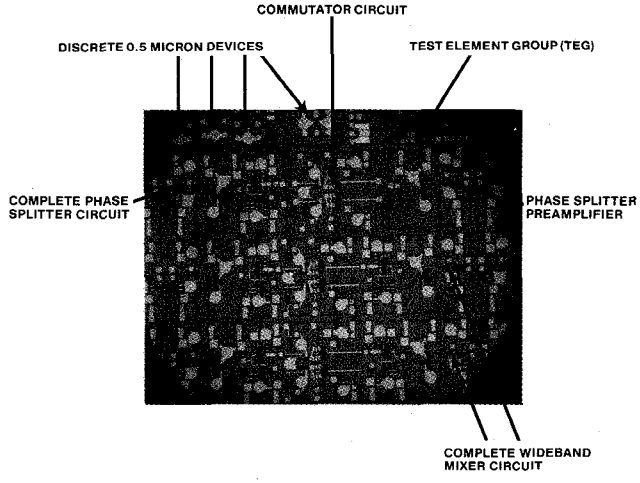

FIGURE 10 PHOTOGRAPH OF DIE OF WIDEBAND DOUBLE BALANCED MIXER

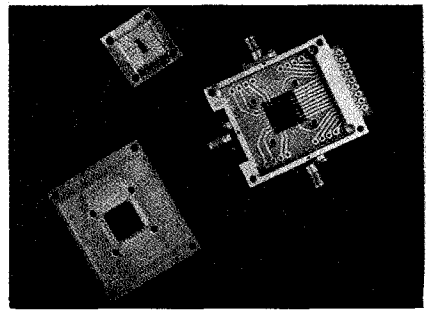

FIGURE 11 PHOTOGRAPH OF DEMOUNTABLE TEST FIXTURE FOR TESTING THE DOUBLE BALANCED MIXER